AMENDMENTS TO THE CLAIMS:

Claims 1-19 (canceled)

20. (Currently Amended) A variable delay circuit comprising:

a first delay circuit having a plurality of first delay stages connected in cascade and receiving an input signal at the initial stage of said first delay stages;

a second delay circuit having a plurality of second delay stages identical to said first delay stages, connected in cascade and receiving a first timing signal at the initial stage of said second delay stages;

a detecting circuit receiving a second timing signal asynchronous to the first timing signal, and detecting, of delayed timing signals outputted from each of said second delay stages, a delayed timing signal having a transition edge near to a ~~the~~ transition edge of the ~~a~~ second timing signal; and

a selecting circuit selecting a delayed signal outputted from said first delay stage corresponding to said second delay stage outputting said delayed timing signal detected by said detecting circuit.